ABSTRACT

The digital phase locked loop circuit according to the invention includes a GAC circuit (4) for calculating the average frequency of the phase locked sampling clock signals in selected channels and for feeding back the calculated average to the phase locked loop. The GAC circuit (4) includes comparators (11_1~11_8) for comparing the frequency of the sampling clock signals in each channel with an allowable frequency range and for outputting a frequency error signal with respect to any channel in which the frequency of the sampling clock signals is outside the allowable frequency range.